Remarks

The above Amendments and these Remarks are in reply to the outstanding Office Action. Claims 1-37 are presently pending. Claims 1, 3-4, 7, 9-11, 13-16, 23-26 and 35-37 have been amended.

Claims 10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 24-25 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As suggested by the Examiner, claim 24 has been amended and therefore claim 24 and dependent claim 25 are believed allowable.

Claims 26-29, 31-32 and 34 are rejected under 35 U.S.C. §102(b) as being anticipated by *Fayneh et al.* (U.S. Patent No. 6,329,882).

Claims 1-9, 11-13, 15-23, 26-28 and 30-37 are rejected under 35 U.S.C. §102(e) as being anticipated by *Dietl et al.* (U.S. Patent No. 6,556,088).

I. Rejection of Claims 26-29, 31-32 and 34 under 35 U.S.C. §102(b)

Claims 26-29, 31-32 and 34 are rejected under 35 U.S.C. §102(b) as being anticipated by *Fayneh et al.*

A. Claim 26

Independent claim 26 calls for "providing a bias current to a circuit component..."

The Examiner in the Office Action at page 3 stated "Fayneh et. al. discloses in figure 2...providing a bias current VBN to a circuit component..." (Emphasis added.)

However, *Fayneh et al.* does not teach "providing a bias current to a circuit component" as is recited in claim 26. Instead, Fayneh et al. discloses providing "bias voltage V_{BN} 226..." from "bias generator 210." Col. 2, lines 19-23 (Emphasis added).

The instant Application, among other things, discloses a PLL/DLL circuit, in an embodiment, that is provides a bias current. In an example, the instant Application discloses the issues relating to voltage biasing PLL/DLLs:

> However, voltage biasing PLL/DLLs by distributing a voltage to various components has many disadvantages. First, voltage biasing PLL/DLLs may not have adequate bandwidth tracking for particular applications. A bias-generating device, such as a metal-oxide field-effect transistor ("MOSFET"), in the various PLL/DLL components receiving the biasing voltage typically must have the same threshold voltage V_T as the matching device generating the bias voltage. If the devices are not the same, mismatch is introduced.

Also, a voltage bias-generating device typically must operate in a saturation region in order for a good matching. Under certain device operation conditions, such as a slow corner, voltage bias-generating devices will not be in a saturation region. Application, page 2, lines 6-15.

B. Claims 27-29, 31-32 and 34

Claims 27-29, 31-32 and 34 are at least patentable for the reasons stated above in regard to independent claim 26.

Further, claim 32 calls for "the circuit component is a phase mixer" which is not described in *Fayneh et al.* Phase detector 202 as described in *Fayneh et al.* is not a claimed "phase mixer." Also," bias voltage V_{BN} 226" is not provided to phase detector 202.

Further, claim 34 calls for "the circuit component is a clock buffer" which is not described by *Fayneh et al.* Divider 228 as described in *Fayneh et al.* is not a claimed "clock buffer." Also, "bias voltage V_{BN} 226" is not provided to divider 228.

It is respectfully requested the Examiner withdraw the rejection of claims 26-29, 31-32 and 34 under 35 U.S.C. §102(b).

II. Rejection of Claims 1-9, 11-13, 15-23, 26-28 and 30-37 under 35 U.S.C. §102(e)

Claims 1-9, 11-13, 15-23, 26-28 and 30-37 are rejected under 35 U.S.C. §102(e) as being anticipated by *Dietl et al.*

A. Claims 1 and 4

Claim 1 calls for "a first circuit to provide a current representing frequency" and "a second circuit ... to provide a bias current in response to the current."

In rejecting claims 1 and 4, the Examiner stated *Dietl et al.* discloses "a voltage regulator 95 for providing a current VBN representing a frequency an VCO 212 [sic, 96] coupled to the voltage generator for providing a bias current V..." However, V is not a current, but a voltage provide by VCO [voltage controlled oscillator] 96. *Dietl et al.* states "a bias generator 95 which generates the two bias voltages VBN and VBP and passes them on to the individual inverter differential stages of the ring oscillator 96 [or VCO 96]." (Emphasis added) Col. 9, lines 9-19.

Further, the Examiner has not identified where *Dietl et al.* describes that voltage VBN "represent[s] frequency" as called for in claim 1 or "a delay" as required in claim 4.

B. Claims 2-3 and 5-6

Dependent claims 2-3 and 5-6 depend from claims 1 and 4 and are at least patentable for similar reasons stated above in regard to claims 1 and 4.

Further, claims 3 and 6 state "the bias current is provided to ...a charge pump, [loop resistor], phase mixer, amplifier, clock buffer..." However, voltage V is provided to divider 97 or phase detector 90, and not the claimed circuit components.

C. Claim 7

In rejecting claim 7, the Examiner has improperly used inconsistent reasoning in rejecting claim 7 and claim 1. In rejecting claim 7, the Examiner stated "the voltage regulator includes a bias-generating device (see component 52 of figure 5) capable of producing a bias current VBN..." However as seen above, the Examiner stated that voltage V provided by VCO 96 of *Dietl et al.* is the claimed "bias current." Further, voltage VBN is a voltage and not the claimed "biasing current."

D. Claims 8-9

Claims 8 and 9 depend from claim 7 and therefore are patentable for at least the reasons stated above in regard to claim 7.

E. Claim 11

In rejecting claim 11, the Examiner stated "the scope of the claims are similar to claims 7-9. Therefore, they are rejected for the same reasons set forth above." The Applicant's attorney respectfully disagrees. Claim 11 calls for "a delay locked loop circuit" and "a voltage-controlled delay line" which is not called for in claims 7-9. The Examiner has not identified these components in the cited art.

F. Claims 12-13

Claims 12 and 13 depend from claim 7 and therefore are patentable for at least the reasons stated above in regard to claim 7.

G. Claim 15

In rejecting claim 15, the Examiner stated that Fig. 9 discloses "...a first circuit 94...and a second circuit 95, coupled to the first circuit, capable of providing a bias current VBN to the first circuit..."

The applicant's attorney respectfully disagrees. Claim 15 is patentable for at least the reasons stated above in regard to claim 7. Also, voltage VBN is not provided to circuit component 94, but to VCO 96, charge pump 91 and charge pump 92.

H. Claims 16-23

Claims 16-23 depend from claim 15 and therefore are patentable for at least the reasons stated above.

Also once again, the Examiner has used inconsistent reasoning in rejecting claim 23. In rejecting independent claim 15, the Examiner stated that "the first circuit" corresponds to circuit component 94 of *Dietl et al.* However, in rejecting dependent claim 23, the Examiner stated that VCO 96 discloses "the first circuit..."

I. Claim 26

Claim 26 is patentable for at least the reasons stated above in regard to claims 1 and 15.

J. Claims 27-28 and 29-34

Claims 27-28 and 29-34 depend from claim 26 and therefore are patentable for at least the reasons stated above in regard to claim 26.

K. Claim 35

Claim 35 is at least patentable for reasons similar to those stated in regard to claims 1 and 26.

L. Claim 36

Claim 36 calls for "obtaining a current representing a delay from a voltage regulator in a delay locked loop circuit" that the Examiner has not identified in the cited art.

M. Claim 37

In rejecting claim 37, the Examiner stated "the scope of claim [37] is similar to claim 15. [T]herefore, it is rejected for the same reason set forth above." The applicant's attorney respectfully disagrees that the scope of the claims 15 and 37 are the same. Claim 15 calls for "a second circuit" and claim 37 calls for "means...to provide a bias current..." Claim 15 calls for a "feedback signal" and claim 37 calls for "an input

signal." Also, voltage VBN is not provided to circuit component 94 (as stated by the Examiner in regard to claim 15), but to VCO 96, charge pump 91 and charge pump 92 of *Dietl et al.*

It is respectfully requested the Examiner withdraw the rejection of claims 1-9, 11-13, 15-23, 26-28 and 30-37 under 35 U.S.C. §102(e).

III. Art Made of Record and Not Relied Upon

Applicant's attorney has reviewed the art made of record and not relied upon and believes this art is no more relevant than the art relied upon by the Examiner.

IV. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-37 is respectfully requested.

Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: September 16, 2005

By: _____ 9/16/05

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